Inventor: Ronald A. Weiner et al.

Title: Methods of Forming Deuterated Silicon Nitride-Containing Materials

Assignee: Micron Technology, Inc.

INFORMATION DISCLOSURE STATEMENT

References – See Attached Form PTO-1449

The citations listed, copies attached, may be material to the examination of the subject application and are therefore submitted in compliance with the duty of disclosure defined in 37 CFR § 1.56. The Examiner is requested to make these citations of official record in this application. No admission is made regarding whether all the submitted references are prior art.

The listed references are discussed in the specification under the heading "Background of the Invention".

The materials cited are presented to assist in and expedite examination of this application. The present invention is considered to be patentable over the cited materials. Expeditious examination and allowance of this application as a patent are therefore urged in order that the public may benefit from the disclosure and commercialization of the invention.

Respectfully submitted,

Dated: 7/3/03

Attorney: _____
David G. Latwesen, Ph.D.
Reg. No. 38,533

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. MI22-2263	SERIAL NO. Filed Herewith
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT Ronald A. Weimer et al.	
		FILING DATE Filed Herewith	GROUP Unknown

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
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	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		*Improved Hot-Electron Reliability in High-Performance, Multilevel-Metal CMOS Using Deuterated Barrier-Nitride Processing;* W.F. Clark et al; IEEE Electron Device Letters, Vol. 20, No. 10, pps. 501-503, October 1999.
	AS		*Realization of High Performance Dual Gate DRAMs without Boron Penetration by Application of Tetrachlorosilance Silicon Nitride Films;* Masayuki Tanaka et al.; 2001 Symposium VLSI Technology Digest of Technical Papers, pps. 123-124

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.